jc715 U.S. PTO
07/21/00

BIRCH, STEWART, KOLASCH & BIRCH, LLP

INTELLECTUAL PROPERTY LAW
8110 GATEHOUSE ROAD
SUITE 500 EAST
FALLS CHURCH, VA 22042-1210
U S A
(703) 205-8000

FAX (703) 205-8050
(703) 698-8590 (G IV)

e-mail mailroom@bskb.com
web http://www.bskb.com

CALIFORNIA OFFICE
COSTA MESA, CALIFORNIA

TERRELL C. BIRCH
RAYMOND C. STEWART
JOSEPH A. KOLASCH
JAMES M. SLATTERY
BERNARD L. SWEENEY*
MICHAEL K. MUTTER
CHARLES GORENSTEIN
GERALD M. MURPHY, JR.
LEONARD R. SVENSSON
TERRY L. CLARK
ANDREW D. MEIKLE
MARC S. WEINER
JOE McKINNEY MUNCY
ROBERT J. KENNEY
DONALD J. DALEY
JOHN W. BAILEY
JOHN A. CASTELLANO, III
GARY D. YACURA

OF COUNSEL
HERBERT M. BIRCH (1905-1996)
ELLIOT A. GOLDBERG*
WILLIAM L. GATES*
EDWARD H. VALANCE
RUPERT J. BRADY (RET.)*
F. PRINCE BUTLER
FRED S. WHISENHUNT

*ADMITTED TO A BAR OTHER THAN VA

THOMAS S. AUCHTERLONIE
JAMES T. ELLER, JR.
SCOTT L. LOWE
MARK J. NUELL, Ph.D.
D. RICHARD ANDERSON
PAUL C. LEWIS
MARK W. MILSTEAD*
JOHN CAMPA*
RICHARD J. GALLAGHER

REG. PATENT AGENTS
FREDERICK R. HANDREN
MARYANNE ARMSTRONG, Ph.D.
MAKI HATSUMI
MIKE S. RYU
CRAIG A. McROBBIE
GARTH M. DAHLEN, Ph.D.
LAURA C. LUTZ
ROBERT E. GOOZNER, Ph.D.
HYUNG N. SOHN
MATTHEW J. LATTIG
ALAN PEDERSEN-GILES
JUSTIN D. KARJALA
C. KEITH MONTGOMERY
TIMOTHY R. WYCKOFF
HERMES M. SOYEZ, Ph.D.
KRISTI L. RUPERT, Ph.D.

jc598 U.S. PTO
09/620014
07/21/00

Date: July 21, 2000
Docket No.: 1152-0263P

Assistant Commissioner for Patents
Box PATENT APPLICATION
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): SAKAGUCHI, Hideaki

For: TESTING DEVICE AND TESTING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUITS

Enclosed are:

X A specification consisting of 38 pages

X 5 sheet(s) of Formal drawings

X An assignment of the invention

___ Certified copy of Priority Document(s)

X Executed Declaration X Original ___ Photocopy

___ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27

___ Preliminary Amendment

___ Information Disclosure Statement, PTO-1449 and reference(s)

___ Other _____

The filing fee has been calculated as shown below:

			LARGE ENTITY			SMALL ENTITY	
FOR	NO. FILED	NO. EXTRA	RATE	FEE		RATE	FEE
BASIC FEE	********** ********** **********	********** ********** **********	***** ***** *****	$690.00	or	**** **** ****	$345.00
TOTAL CLAIMS	11 - 20 =	0	x18 =$	0.00	or	x 9 = $	0.00
INDEPENDENT	4 - 3 =	1	x78 =$	78.00	or	x 39 = $	0.00
MULTIPLE DEPENDENT CLAIM PRESENTED	no		+260 = $	0.00	or	+130 = $	0.00
			TOTAL $	768.00		TOTAL $	0.00

X A check in the amount of $ 808.00 to cover the filing fee and recording fee (if applicable) is enclosed.

___ Please charge Deposit Account No. 02-2448 in the amount of $_____. A triplicate copy of this transmittal form is enclosed.

___ No fee is enclosed.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. 1.16 or under 37 C.F.R. 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____

DONALD J. DALEY
Reg. No. 34,313
P. O. Box 747
Falls Church, Virginia 22040-0747

(703) 205-8000
DJD/dpt

SPECIFICATION

TITLE OF THE INVENTION

TESTING DEVICE AND TESTING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a testing device and testing method for a semiconductor integrated circuit (e.g., a LCD driver IC, etc.) that incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via the associated output terminals, and particularly relates to a testing device and testing method which can examine the output voltages from the D/A converters, very quickly with high accuracy.

(2) Description of the Prior Art

With the development of LCD panels into a high precision configuration, LCD driver LSIs incorporated in LCD panels have become developed to deal with a greater number of outputs and a greater number of tones. For such tonal display, each output circuit in the LCD driver LSI incorporates its own D/A converter to output a tonal voltage. For example, a 6 bit D/A converter can display 64 levels of tones while a 8 bit D/A converter can display 256 levels of tones.

Upon the test for such a LCD driver LSI, it is checked if all the tonal voltage levels output from individual D/A converters fall within respective correct ranges and if the values of a tonal voltage level for all D/A converters meet the predetermined uniformity.

Fig.1 is a conceptual view illustrating a conventional testing method by using a test example of a LCD driver LSI incorporating 'm' output DA converts each having 'n' tonal levels.

A semiconductor testing device (tester) is used to supply an input signal to an LCD driver LSI 51 so that each D/A converter 52 outputs a voltage level corresponding to the first tonal level. The voltage levels corresponding to the first tonal level are output from associated output terminals (Y1, ···, Ym) of LCD driver LSI 51 and input to input channels (1ch, ···, mch) of tester 53. In tester 53, matrix switches 54 are sequentially turned on and off so that the outputs corresponding to the first tonal level are sequentially measured from the first output to the m-th output, one by one, using a high accuracy analog voltage measuring device 55 incorporated in the tester. The measured results are sequentially stored in an incorporated data memory 56. This process is repeated for 'n' tonal levels until all pieces of data relating to all the outputs (m outputs) for all tonal levels (n levels) can be stored into memory 56. As a result,

m x n pieces of data will be stored into memory 56. The data stored in this memory 56 is subjected to a series of logical and arithmetical operations through an unillustrated processing unit incorporated in tester 53 so as to check each tonal voltage value of each output and the uniformity of each tonal voltage level between all the outputs.

In such a test of a LCD driver LSI 51, with the development towards a greater number of outputs and a greater number of tones, the amount of data to be picked up and the time required for data processing increase, so that the testing time increases sharply. Further, increase of the tonal levels in number requires a greater precision for measuring the voltage of each tonal level, needing a further longer testing time and also an expensive semiconductor testing device incorporating a high precision voltage measuring device.

As stated above, as LCD driver LSIs have become developed to deal with a greater number of outputs and a greater number of tones, the conventional testing method needs a much longer testing time and also needs an expensive semiconductor testing device incorporating a high precision voltage measuring device. Thus, the test cost is increasing more and more.

As a conventional semiconductor testing device to solve the above problems, Japanese Patent Application Laid-Open

Hei 9 No.312569 has proposed a semiconductor testing device.

Fig.2 is a block diagram showing the configuration of the semiconductor testing device disclosed in Japanese Patent Application Laid-Open Hei 9 No.312569.

That is, the D/A converter testing device of this disclosure includes: a digital signal generator 60 for generating n-bit digital data; a clock generator 61; a D/A converter DUT 62 of a device under test which receives the data from digital signal generator 60 and a clock signal from clock generator 61 and outputs an analog signal Vg; a reference (REF) D/A converter 63 which receives the data branched from digital signal generator 60 and the clock signal branched from clock generator 61 and outputs a reference voltage Vref; a differential amplifier 64 receiving the output from D/A converter DUT 62 of the device under test at its one input and the output from reference D/A converter 63 at the other input to effect differential amplification; and a dual comparator 65 which receives the differential amplification output from differential amplifier 64 and checks if the signal in question falls in the allowable range between the upper and lower boundaries. With the above configuration, it is possible to provide a D/A converter testing device that provides a high throughput.

However, the semiconductor testing device (D/A converter testing device) disclosed in Japanese Patent

Application Laid-Open Hei 9 No.312569 has suffered from the following difficulties. That is, in the D/A converter testing device shown by Japanese Patent Application Laid-Open Hei 9 No.312569, since the same signals are input to both D/A converter DUT 62 of the device under test and reference D/A converter 63, it is necessary to use a non-defective D/A converter of the device under test for reference D/A converter 63. This is because the number of terminals is different depending upon the number of tones reproduced by the D/A converter of the device under test. Therefore, if a different type of D/A converter is to be tested, there is a need to have an extra non-defective D/A converter of the same type as the D/A converter as a reference D/A converter. That is, the difficulties of the testing device shown by Japanese Patent Application Laid-Open Hei 9 No.312569 is that there is a need to have a non-defective high-quality reference D/A converter for each type of D/A converter of the device to be tested or for each type of semiconductor integrated circuit incorporating a D/A converter to be tested.

SUMMARY OF THE INVENTION

The present invention has been completed in view of the above prior art difficulties, and it is therefore an object of the present invention to provide a testing device and

testing method for semiconductor integrated circuits which can markedly reduce the test time and enables a conventional inexpensive testing device to perform highly accurate testing without the necessity of providing a separate reference voltage generator for each type of semiconductor integrated circuits to be tested.

In order to achieve the above object, the present invention is configured as follows:

In accordance with the first aspect of the present invention, a testing device for a semiconductor integrated circuit which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, includes:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output

voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range.

In accordance with the second aspect of the present invention, the testing device for semiconductor integrated circuits having the above first feature is characterized in that the reference voltage generator is a D/A converter which receives a digital data signal different from that of the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal.

The third aspect of the present invention resides in a testing method for a semiconductor integrated circuit which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and

can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output

from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range.

In accordance with the fourth aspect of the present invention, the testing method for semiconductor integrated circuits having the above third feature, comprises the above first through third steps and is characterized in that even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

In accordance with the fifth aspect of the present invention, the testing method for semiconductor integrated circuits having the above third feature, further comprises:

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range; and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals fall within the second given voltage range,

and is characterized in that the fourth and fifth steps are repeated until the judgment at the fifth step changes.

In accordance with the sixth aspect of the present invention, the testing method for semiconductor integrated circuits having the above fifth feature is characterized in that, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

In accordance with the seventh aspect of the present invention, the testing method for semiconductor integrated circuits having the above fifth feature is characterized in that the width of the second given range is made narrower as the above fourth and fifth steps are repeated.

The eighth aspect of the present invention resides in a storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively outputs multiple sets of reference voltages required for testing multiple kinds of semiconductor

integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from

the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

The ninth aspect of the present invention resides in a storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively outputs multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output

voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step;

the third step for judging at one time whether all the amplified differential values obtained in the second step

in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage;

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range; and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals falls within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.

In accordance with the tenth aspect of the present invention, the storage medium for storing the program for a computer to execute the testing method for semiconductor integrated circuits having the above ninth feature is characterized in that, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

In accordance with the eleventh aspect of the present invention, the storage medium for storing the program for

a computer to execute the testing method for semiconductor integrated circuits having the above ninth feature is characterized in that the width of the second given range is made narrower as the above fourth and fifth steps are repeated.

According to the testing device and testing method for semiconductor integrated circuits of the present invention, the output voltage output from the output terminal of each D/A converter in a semiconductor integrated circuit is compared to the reference voltage in each differential amplifier. The results, i.e., the amplified output voltages from the individual differential amplifiers are input in parallel to a comparator. In the comparator, it is judged as to whether the amplified output voltage from each of the differential amplifiers falls within the given voltage range.

According to the testing device and testing method for semiconductor integrated circuits of the present invention, it is possible to markedly reduce the test time by using a comparator which effects simultaneous judgements of all the amplified output voltages, in testing a semiconductor integrated circuit such as a LCD driver LSI which has been developed to deal with a greater number of outputs and a greater number of tones. Further, the testing device of the present invention enables high accuracy testing using a

conventional inexpensive tester without the necessity of a high accuracy analog voltage measuring device for voltage measurement as in the conventional configuration, thus making it possible to sharply reduce the testing cost. It is possible to classify the quality of each device based on the variation in voltage output, so that applications of the LCD panel to which the device is applied can be enlarged, thus making it possible to improve the production yield and reducing LCD drivers to fair price. Further, since the reference voltage generator is commonly used for testing multiple kinds of semiconductor integrated circuits, it is no longer necessary to provide a separate reference voltage generator for each type of semiconductor integrated circuit under test. Consequently, the present invention enables only a single testing device to achieve efficient testing of multiple kinds of semiconductor integrated circuits.

The width of the first given voltage range is made narrower by a multiple of the predetermined voltage width to set up a second given voltage range, and it is judged at the same time whether all the differential amplified values from all the associated output terminals fall within the second given voltage range. The devices under test are classified into multiple ranks, based on the second given voltage range which is determined by checking the change in the pass/reject judgement result. Therefore, it is

possible to classify the quality of each device based on the variation in voltage output, so that usage of the LCD panel to which the device is applied can be enlarged, thus making it possible to improve the production yield and reducing LCD drivers to fair price.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a block diagram showing the configuration of a conventional testing device;

Fig.2 is a block diagram showing the configuration of another conventional testing device;

Fig.3 is a block diagram showing a configuration of a LCD driver LSI testing device in accordance with one embodiment of the present invention;

Fig.4 is a voltage waveform chart for illustrating the operation of the same embodiment;

Fig.5 is a block diagram showing the configuration of the converter shown in Fig.3;

Fig.6 is a flowchart showing the operation of the same embodiment;

Fig.7 is an illustrative view showing the scheme for narrowing down the first given voltage range in accordance with a second embodiment of the present invention; and

Fig.8 is a flowchart showing the operation of the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will hereinafter be described in detail with reference to the embodiments of the invention.

Fig.3 is a block diagram showing a configuration of a LCD driver LSI testing device in accordance with one embodiment of the present invention. Fig.3 shows a case where m-output, n-tonal LCD driver LSI is tested. Fig.4 is a voltage waveform chart for illustrating the operation of the testing device shown in Fig.3.

A LCD driver LSI 1 has m output terminals 3. Each output terminal 3 is connected to the output terminal of an associated D/A converter 2. Each D/A converter 2 outputs a tonal voltage for n-levels of tones. The tonal voltage outputs from all output terminals 3 are supplied in parallel to a differential amplifier module array 4 made up of a number of differential amplifiers 5. More specifically, each of the tonal voltage outputs is input to one of the two inputs to the associated differential amplifier 5.

Designated at 8 is a voltage generator for sequentially generating n-levels of reference voltages (expected voltages) to be compared to the aforementioned tonal voltages. The expected voltage output from voltage generator 8 is output to a common input terminal 7 which is input to the other terminals of all differential amplifiers 5 constituting

differential amplifier array module 4. This reference voltage generator 8 is configured so as to be able to be commonly used for testing of different kinds of LCD driver LSIs, each having different D/A converter's tonal output level sets from others. More specifically, the reference voltage generator is able to generate a multiple number of tonal voltages, in increments of Vmin, a predetermined, smallest voltage step, in accordance with the input digital data, and is able to sequentially generate the desired tonal voltages when multiple pieces of digital data corresponding to the standard multiple tonal voltages to be output from a LCD driver LSI 1 under test are selected and sequentially supplied to the reference voltage generator. That is, selection of the digital data supplied to this reference voltage generator 8 enables free generation of a different set of reference voltages required for LCD driver LSIs 1 of a desired type. Alternatively, the reference voltage generator may also be configured in the following manner. That is, if all the sets of the tonal voltages to be output from D/A converters incorporated in different types of semiconductor integrated circuits to be tested by the testing device having the reference voltage generator are known, it is possible to configure the reference voltage generator so as to be able to output all the tonal voltages in accordance with the input digital data signal (in this case, the voltage

difference between adjacent output reference voltages is not always constant, differing from the above configuration). Thereby, it is possible to configure a reference voltage generator which can selectively generate multiple sets of reference voltages, required for testing of the multiple kinds of semiconductor integrated circuit.

As shown in Fig.4, each differential amplifier 5 produces an amplified output voltage which is obtained by amplifying the voltage deviation of a tonal voltage 13 output from LCD driver LSI 1 from an expected voltage 14 output from voltage generator 8 (e.g., V1, V2 and V3, shown in Fig.4) by a given ratio (e.g., 100 times or greater). This amplifying process of the voltage deviation by means of differential amplifiers 5 assures high precision in the comparing judgement in a subsequent comparator 12. The above amplified output voltages are output from differential amplifiers 5 via output terminals 9, which are connected to associated input channels 11 of a tester 10, so that each amplified output voltage is input to tester 10. A comparator 12 as a part of tester 10 checks all the amplified output voltages, at the same time, judging whether the amplified output voltage supplied from each differential amplifier via associated input channel 11 falls within the given range (for example, whether the voltage deviation falls within the range of $\pm$20 mV, for 64 tones, and within the range of $\pm$5 mV, for

256 tones), and outputs a judgement signal which indicates that all the input voltages fall within the associated voltage ranges or that any of the input voltages falls outside the predetermined range.

Fig.5 shows a block diagram of this comparator 12. In this figure, 15 designates a voltage comparator, 16 and 17 are both AND circuits. VH is the upper limit voltage of the given voltage range and VL is the lower limit voltage of the given voltage range. In this configuration, if all the amplified output voltages supplied from differential amplifiers 5 fall within the given voltage range, AND circuit 17 produces the H-level output. If one of the amplified output voltages falls output the given voltage range, AND circuit 17 produces the L-level output.

The testing device of the present embodiment can be realized by adding only a differential amplifier array module 4 and a voltage generator 8 to a conventional tester 10 of a built-in comparator type. That is, combination of only some small devices with the existing device enables provision of a markedly useful testing device which can effect high accurate testing in a short period.

The operation of the testing device of the present embodiment will be described hereinbelow. Fig.6 is a flowchart showing the operation of this embodiment.

To begin with, LCD driver LSI 1 is set and operated so

that the tonal voltage representing the first tone is output from 'm' output terminals 3 (S1). The tonal voltages output from 'm' output terminals 3 are input in parallel to associated differential amplifiers 5 through their input terminals 6, one of the two being input to each differential amplifier. Voltage generator 8 is controlled, as it is supplied with the predetermined digital data signal, so as to generate an expected voltage corresponding to the first tonal voltage in LCD driver LSI 1 under test (S2). This expected voltage is input to the other input terminal (common input terminal) 7 of each differential amplifier 5.

At S3, each differential amplifier 4, based on the associated input voltage, calculates the difference between the first tonal voltage output from the associated terminal of LCD driver LSI 1 and the expected voltage (S3) and amplifies the calculation by a given magnification (e.g., 100 times or greater)) so as to produce a voltage-amplified output voltage (S4). The voltage-amplified output voltages from all amplifiers 4 are input in parallel to tester 10, in which a given voltage range has been set up (S5). In comparator 12 of tester 10, it is judged whether each voltage-amplified output voltage falls within the given voltage range (S6). In this judgement, when AND circuit 17 produces the L-level output, which means that any of the output voltages is judged to fall out of the given range, the testing operation is

stopped at that point so that the LSI under test is rejected as a defective (S7). On the contrary, when AND circuit 17 produces the H-level output, which means that all the output voltages are judged to fall within the given voltage range, the operation goes to the next step, i.e., the test on the second tonal voltage level (S8).

Specifically, LCD driver LSI 1 is operated so as to output the tonal voltage representing the second tone from 'm' output terminals 3 (S1). The tonal voltages output from 'm' output terminals 3 are input in parallel to associated differential amplifiers 5 through their input terminals 6, one of the two input to each differential amplifier. Voltage generator 8 is set and controlled, as it is supplied with the predetermined digital data signal, so as to generate an expected voltage 14 corresponding to the second tonal voltage 13 in LCD driver LSI 1 under test (S2). This expected voltage is input to the other input terminal (common input terminal) 7 of each differential amplifier 5. Each differential amplifier 5, based on the associated input voltage, calculates the difference between the second tonal voltage output from the associated terminal of LCD driver LSI 1 and the expected voltage (S3(the first step)) and amplifies the calculation by a given magnification (e.g., 100 times or greater)) so as to produce a voltage-amplified output voltage (S4(the second step)). The voltage-amplified output

voltages from all amplifiers 4 are input in parallel to tester 10, in which a given voltage range has been set up (S5). In comparator 12 of tester 10, it is judged whether each voltage-amplified output voltage falls within the given voltage range (S6(the third step)). In this judgement, when AND circuit 17 produces the L-level output, which means that any of the output voltages is judged to fall out of the given range, the testing operation is stopped at that point so that the LSI under test is rejected as a defective (S7). On the contrary, when AND circuit 17 produces the H-level output, which means that all the output voltages are judged to fall within the given voltage range, the operation goes to the next step, i.e., the test on the third tonal voltage level (S8).

The same test will be repeated until the test on the n-th tonal voltage is completed. Thus, it is possible to check all the tonal voltages output from individual D/A converters incorporated in the LCD driver LSI.

Next, another embodiment according to the present invention will be described.

Tonal voltage waveform 13 output from LCD driver 1 having a plurality of DACs presents voltage deviations V1, V2 and V3 with respect to the expected voltage waveform 14, as shown in Fig.4. These deviations are attributed to the voltage deviation at the output voltage from individual DACs 2 in

LCD driver 1. Detection of the amount of voltage deviation also takes an important role in the LCD driver test.

In the conventional scheme, all the levels of the tonal voltages are first determined by the high-precision analog measuring device and these values are subjected to the predetermined arithmetic operation in the tester so as to determine the variations in voltage. However, according to the former embodiment, the differential voltages output from differential amplifiers 5 are input to comparator 15 where each input is always compared with constant voltages VH and VL set therein. In contrast, in the present embodiment, the levels of these VH and VL are adapted to be varied individually, so that the voltage difference between the level on the VH side at which the device under test will translate from the pass to the reject and the level on the VL side at which the device under test will translate from the pass to the reject can thereby be determined.

Now a specific embodiment will be described referring to actual numerals.

In the example of the numeric measurement shown in Fig. 7, it is checked whether all the outputs corresponding to an ideal value fall within the range between VOH = 2V and VOL = 1V. The present embodiment provides a further detailed evaluation of the devices (VOH = 2 V, VOL = 1 V: the first given voltage range).

First, VOH is varied from 2 V with decrements of 0.1 V so as to detect the point at which the device under test becomes rejected. That is, the maximum value or the farthest value from the ideal value among all the pins becomes the 'reject' point, and suppose pin 2 shown in Fig.7 has the maximum value, VOH =1.86V is determined as the 'reject' point.

In a similar manner, VOL is varied from 1 V with increments of 0.1 V so as to detect the point at which the device under test becomes rejected.

In this case, the minimum value or the farthest value from the ideal value among all the pins becomes the 'reject' point, and suppose pin 1 shown in Fig.7 has the minimum value, VOH =1.24V is determined as the 'reject' point (VOH = 1.86, V VOL = 1.24 V: the second given voltage range). The range from VOL =1.24 V to VOH = 1.86 V detected here represents the variation of all the pins and the devices can be ranked or their usage can be classified according to this value . In the above description, the reference values are varied by steps of 0.1 V, but this varying unit can be made smaller so as to enhance the measuring accuracy. Here, VOH and VOL are set in tester 10.

Fig.8 is a flowchart showing the operation of the present embodiment. This flowchart shows the operation for a single tone, and the same reference numerals are allotted to those corresponding to Fig.6.

This flowchart differs from that of Fig.6, in the steps of S11, S12 and S13. That is, at S6 (the third step), when comparator 12 of tester 10 judges whether each voltage-amplified output voltage falls within the given voltage range and AND circuit 17 produces the H-level output, which means that all the output voltages are judged to fall within the given voltage range, the given voltage range is made narrower to set up a second given range (S11, the fourth step). Then, the operation returns again to S6 (the fifth step), where it is checked as to whether the voltage-applied output voltage falls within the second given voltage range.

Upon the judgement at S6 (the fifth step), when AND circuit 17 produces the L-level output, which means that any of the output voltages is judged to fall out of the predetermined range, the voltage variation of the output voltages from the output terminals is extracted, and based on the obtained voltage variation, the device is ranked (S13).

As S6 and S11 are repeated, the width of the given voltage range is made narrower. In this way, it is possible to rank a semiconductor integrated circuit under test by specifying where in the voltage range the device belongs to.

In the present invention, it is very effective if use is made of a storage medium that stores the program for allowing the computer to perform the above first through fifth testing steps.

As has been detailed heretofore, according to the testing device for semiconductor integrated circuits of the present invention, it is possible to markedly reduce the test time by using a comparator which effects simultaneous judgements of all the amplified output voltages, in testing a semiconductor integrated circuit such as a LCD driver LSI which has been developed to deal with a greater number of outputs and a greater number of tones. Further, the testing device of the present invention enables high accuracy testing using a conventional inexpensive tester without the necessity of a high accuracy analog voltage measuring device for voltage measurement as in the conventional configuration, thus making it possible to sharply reduce the testing cost. It is possible to classify the quality of each device based on the variation in voltage output, so that applications of the LCD panel to which the device is applied can be enlarged, thus making it possible to improve the production yield and reducing LCD drivers to fair price. Further, since the reference voltage generator is commonly used for testing multiple kinds of semiconductor integrated circuits, it is no longer necessary to provide a separate reference voltage generator for each type of semiconductor integrated circuit under test. Consequently, the present invention enables only a single testing device to achieve efficient testing of multiple kinds of semiconductor integrated circuits.

WHAT IS CLAIMED IS:

1. A testing device for a semiconductor integrated circuit which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, comprising:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range.

2. The testing device for semiconductor integrated circuits according to Claim 1, wherein the reference voltage generator is a D/A converter which receives a digital data

signal different from that of the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal.

3. A testing method for a semiconductor integrated circuit which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output

voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range.

4. The testing method for semiconductor integrated

circuits according to Claim 3 comprising the above first through third steps, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

5. The testing method for semiconductor integrated circuits according to Claim 3, further comprising:

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range; and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals fall within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.

6. The testing method for semiconductor integrated circuits according to Claim 5, wherein, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

7. The testing method for semiconductor integrated

circuits according to Claim 5, wherein the width of the second given range is made narrower as the above fourth and fifth steps are repeated.

8. A storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively outputs multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage

range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step; and

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage.

9. A storage medium for storing the program for a computer to execute a testing method for a semiconductor integrated circuits which incorporates a multiple number of D/A converters and outputs voltages from the D/A converters via associated output terminals, wherein a testing device for semiconductor integrated circuits is used which comprises:

a reference voltage generator which generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals and can selectively outputs multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits;

a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from the associated output terminal and the other for receiving the reference voltage from the reference voltage generator; and

a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each of the differential amplifiers falls within a given voltage range, wherein the reference voltage generator includes a D/A converter which receives a digital data signal different from the signals to the D/A converters incorporated in the

semiconductor integrated circuit to generate the multiple number of reference voltages and can selectively output a necessary set of reference voltages from the multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuit, in accordance with the selection of the digital data signal,

the method comprising:

the first step for calculating the difference between the reference voltage generated from the reference voltage generator of the testing device and the output voltage output from each output terminal, for all the output terminals;

the second step for amplifying the values obtained from the first step;

the third step for judging at one time whether all the amplified differential values obtained in the second step in association with respective output terminals fall within the first given voltage range, wherein even if the output from the device under test varies, the first given voltage range can be kept at constant by computing the difference between the output from the device under test and the associated reference voltage generated from the above reference voltage;

the fourth step for decreasing the width of the first given voltage range by a multiple of the predetermined voltage width to set up a second given voltage range; and

the fifth step for judging at one time whether all the amplified differential values associated to respective output terminals falls within the second given voltage range, wherein the fourth and fifth steps are repeated until the judgment at the fifth step changes.

10. The storage medium for storing the program for a computer to execute the testing method for semiconductor integrated circuits according to Claim 9, wherein, based on the value of the second given voltage range when the judgment at the fifth step changes, the devices under test are classified into a plurality of ranks.

11. The storage medium for storing the program for a computer to execute the testing method for semiconductor integrated circuits according to Claim 9, wherein the width of the second given range is made narrower as the above fourth and fifth steps are repeated.

ABSTRACT OF THE DISCLOSURE:

A testing device for LCD driver LSIs, includes: a voltage generator which generates a multiple number of expected voltages to be compared to each output voltage output from each of the output terminals and can selectively output multiple sets of reference voltages required for testing multiple kinds of semiconductor integrated circuits; a multiple number of differential amplifiers, each having two input terminals, one for receiving the output voltage output from each of the output terminals and the other for receiving the reference voltage from the reference voltage generator; and a comparator that receives the amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltage from each differential amplifier falls within the given voltage range.

FIG. 1 PRIOR ART

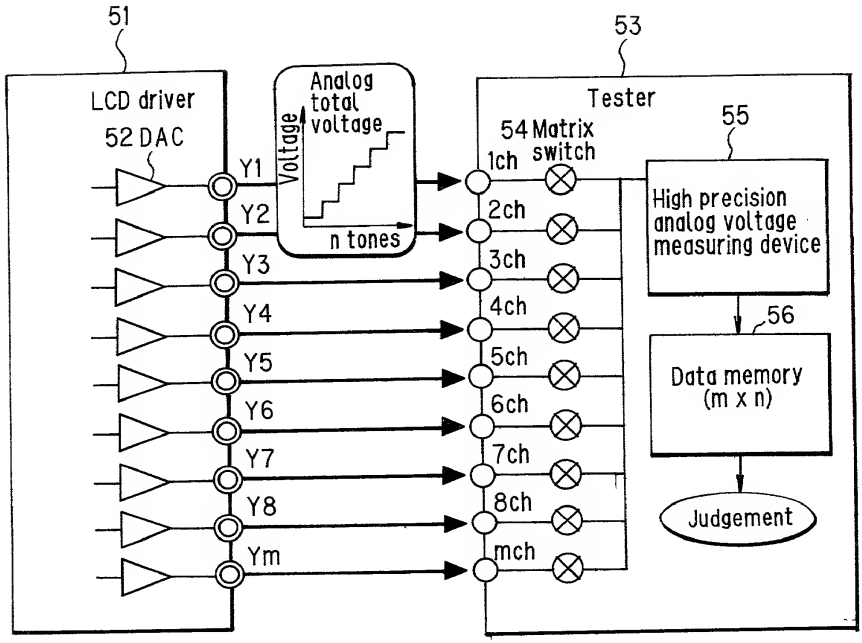


FIG. 2 PRIOR ART

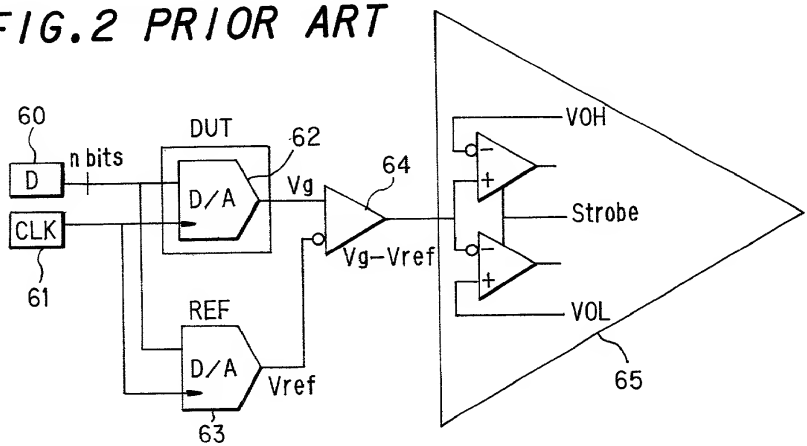


FIG. 3

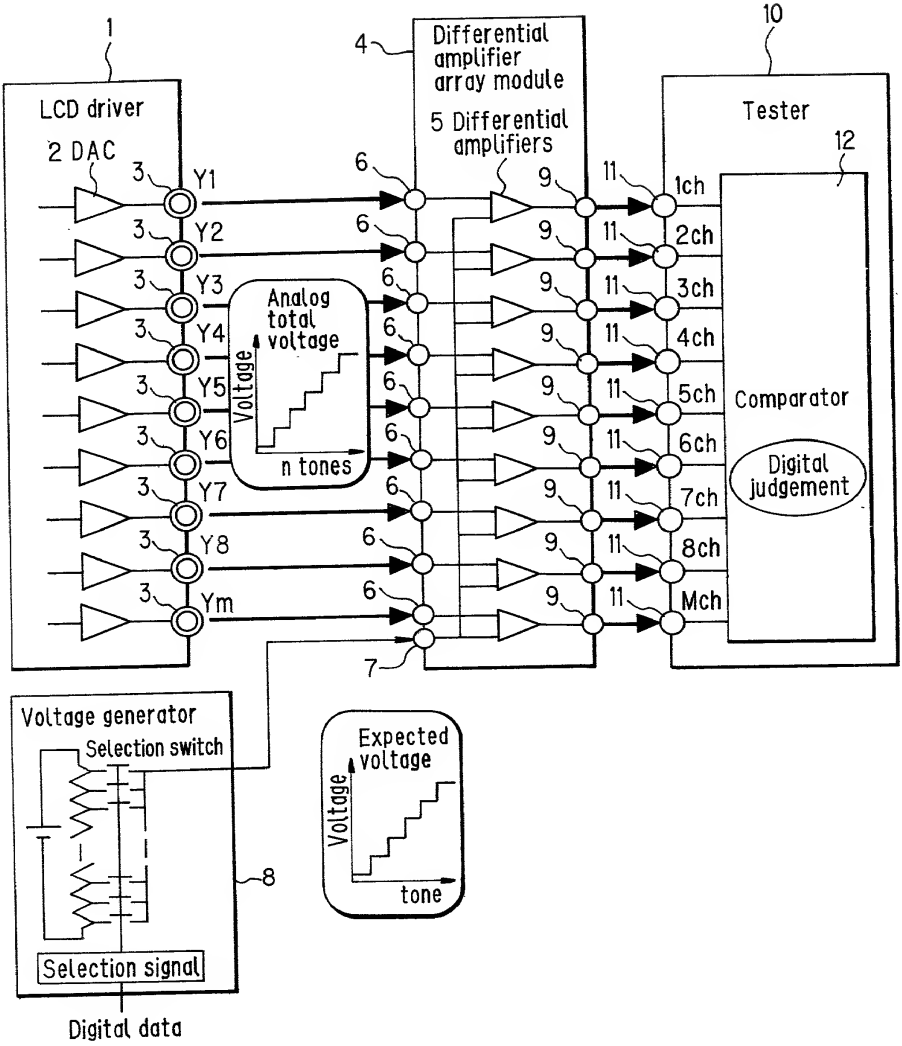

1
LCD driver
2 DAC
3
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Ym
Analog total voltage
Voltage
n tones
4
Differential amplifier array module
5 Differential amplifiers
6
7
9
11
10
Tester
12
1ch
2ch
3ch
4ch
5ch
6ch
7ch
8ch
Mch
Comparator
Digital judgement
Voltage generator
Selection switch
8
Selection signal
Digital data
Expected voltage
Voltage
tone

FIG. 4

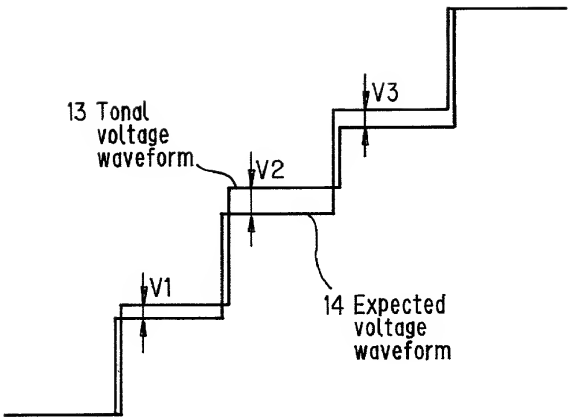

13 Tonal voltage waveform
V1
V2
V3
14 Expected voltage waveform

FIG. 5

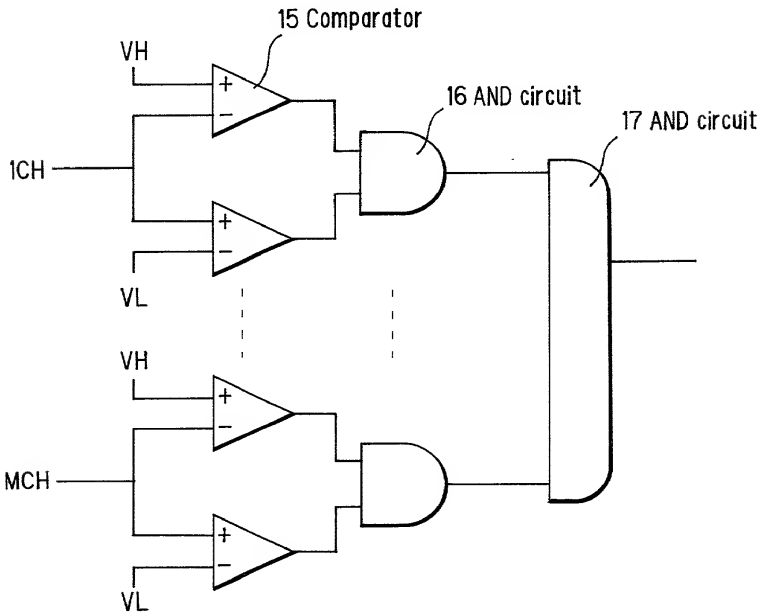

15 Comparator
VH
1CH
VL
16 AND circuit
17 AND circuit
VH
MCH
VL

FIG. 6

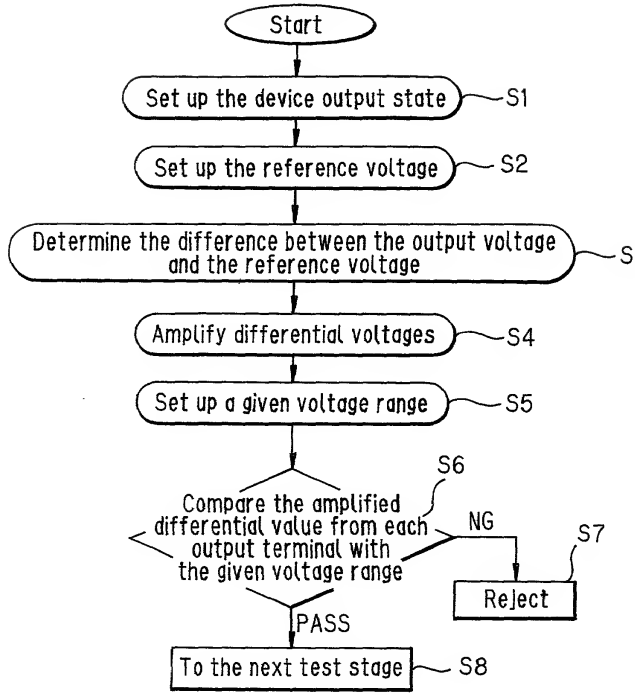

Start
Set up the device output state
S1
Set up the reference voltage
S2
Determine the difference between the output voltage and the reference voltage
S3
Amplify differential voltages
S4
Set up a given voltage range
S5
S6
Compare the amplified differential value from each output terminal with the given voltage range
NG
S7
Reject
PASS
To the next test stage
S8

FIG. 7

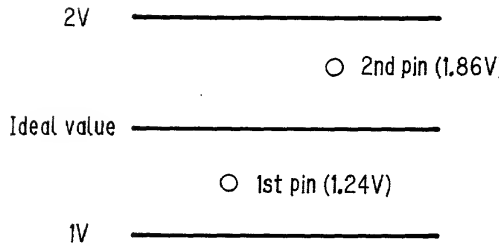
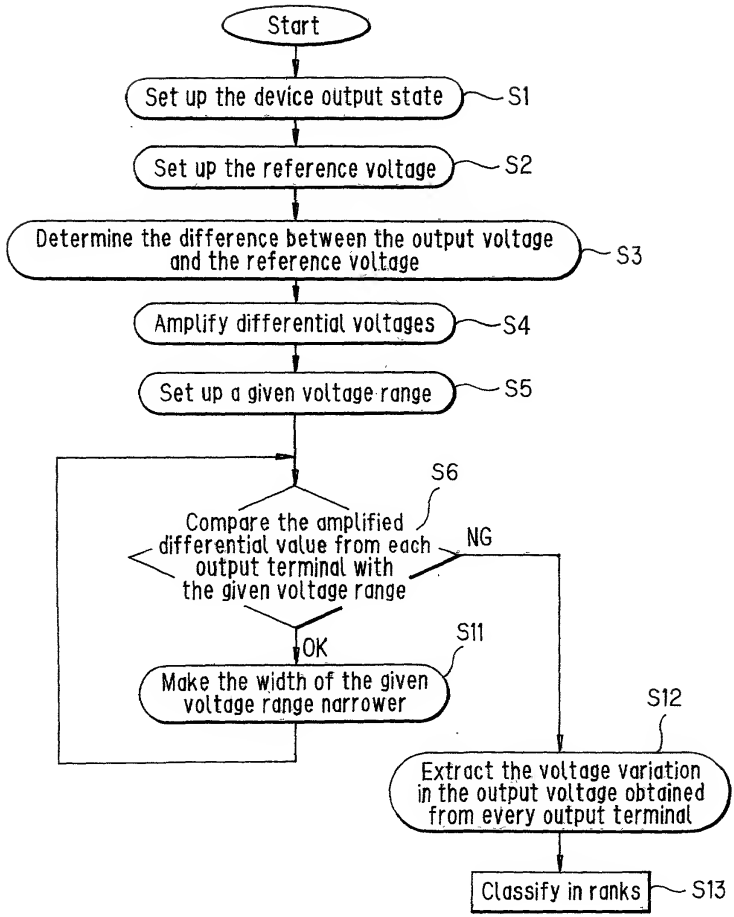

2V
2nd pin (1.86V)
Ideal value
1st pin (1.24V)
1V

FIG.8


Start
Set up the device output state
S1
Set up the reference voltage
S2
Determine the difference between the output voltage and the reference voltage
S3
Amplify differential voltages
S4
Set up a given voltage range
S5
S6
Compare the amplified differential value from each output terminal with the given voltage range
NG
OK
S11
Make the width of the given voltage range narrower
S12
Extract the voltage variation in the output voltage obtained from every output terminal
Classify in ranks
S13

BIRCH, STEWART, KOLASCH & BIRCH, LLP

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO. 1152-0263P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: TESTING DEVICE AND TESTING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUITS

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____; and /or

the specification was filed on _____ as PCT
International Application Number _____; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)

Prior Foreign Application(s) (Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed
Hei 11-208469	Japan	July/23/1999	☒ Yes ☐ No
2000-174119	Japan	June/9/2000	☒ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

Insert Provisional Application(s): (if any)

(Application Number)	(Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

Insert Requested Information: (if appropriate)

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S. Application(s): (if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

1152-0263P

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Terrell C. Birch	(Reg. No. 19,382)	Raymond C. Stewart	(Reg. No. 21,066)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
Leonard R. Svensson	(Reg. No. 30,330)	Terry L. Clark	(Reg. No. 32,644)
Andrew D. Meikle	(Reg. No. 32,868)	Marc S. Weiner	(Reg. No. 32,181)
Joe McKinney Muncy	(Reg. No. 32,334)	Andrew F. Reish	(Reg. No. 33,443)
C. Joseph Faraci	(Reg. No. 32,350)	Donald J. Daley	(Reg. No. 34,313)

Send Correspondence to: **BIRCH, STEWART, KOLASCH & BIRCH, LLP**

P.O. Box 747 • Falls Church, Virginia 22040-0747

Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor:
Insert Name of Inventor
Insert Date This Document is Signed
Insert Residence
Insert Citizenship
Insert Post Office Address

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Hideaki	SAKAGUCHI	Hideaki Sakaguchi	July 7, 2000

Residence (City, State & Country)	CITIZENSHIP
Tenri-shi, Nara, Japan	Japan

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)
135-3, Senzai-cho, Tenri-shi, Nara, Japan

Full Name of Second Inventor, if any:
see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*

Residence (City, State & Country)	CITIZENSHIP

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

Full Name of Third Inventor, if any
see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*

Residence (City, State & Country)	CITIZENSHIP

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

Full Name of Fourth Inventor, if any
see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*

Residence (City, State & Country)	CITIZENSHIP

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

Full Name of Fifth Inventor, if any
see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*

Residence (City, State & Country)	CITIZENSHIP

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

* DATE OF SIGNATURE